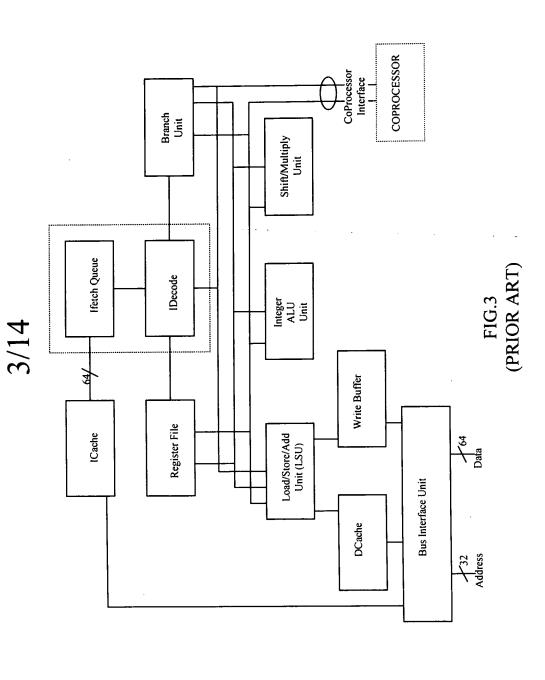
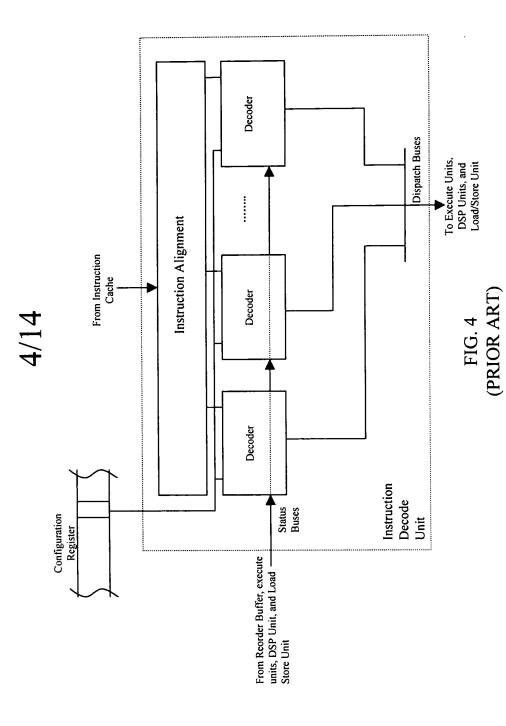


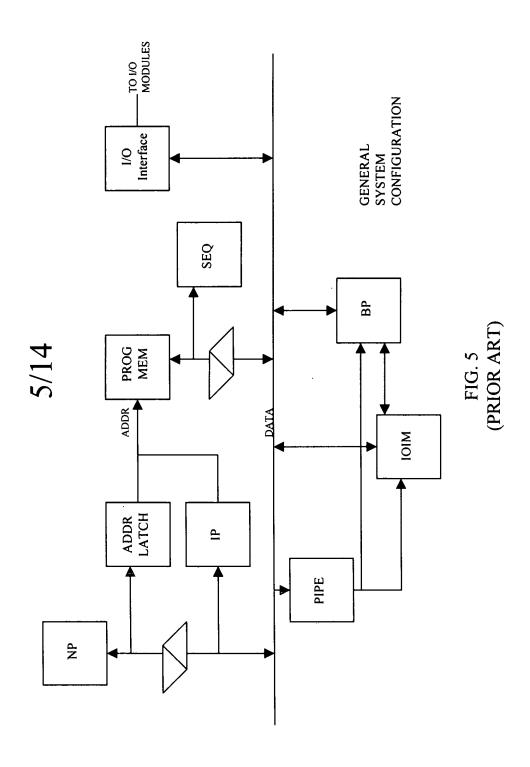
FIG. 1 (PRIOR ART)

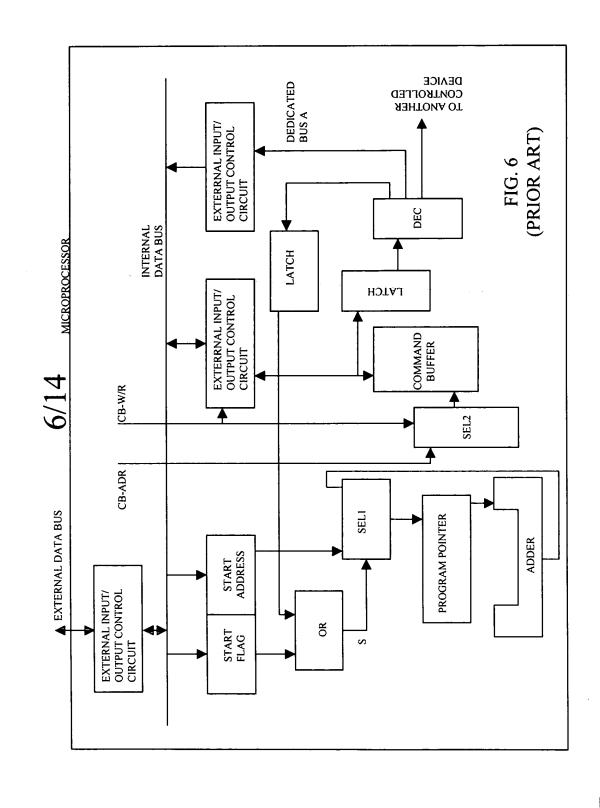
Coprocessor	Compatible Processor	Coprocessor Characteristics
Intel 8087	Intel 8086/8088	5 Mhz, 70 cycles for add & 700 cycles for log
Intel 80287	Intel 80286	12.5 Mhz, 30 cycles for add & 264 cycles for log
Intel 387DX	Intel 386DX	33 Mhz, 12 cycles for add & 210 cycles for log
Intel i486	Intel i486 (same chip)	33 Mhz, 8 cycles for add & 171 cycles for log
Motorola MC68882	Motorola MC68020/68030	40 Mhz, 56 cycles for add & 574 cycles for log
Weitek 3167	Intel 386DX	33 Mhz, 6 cycles for add & 365 cycles for log by software emulation
Weitek 4167	Intel i486	33 Mhz, 2 cycles for add & not available for log

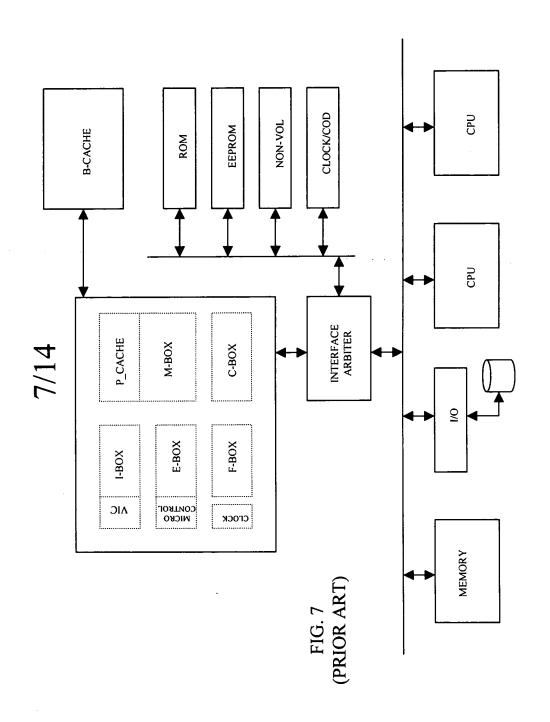
FIG. 2 (PRIOR ART)

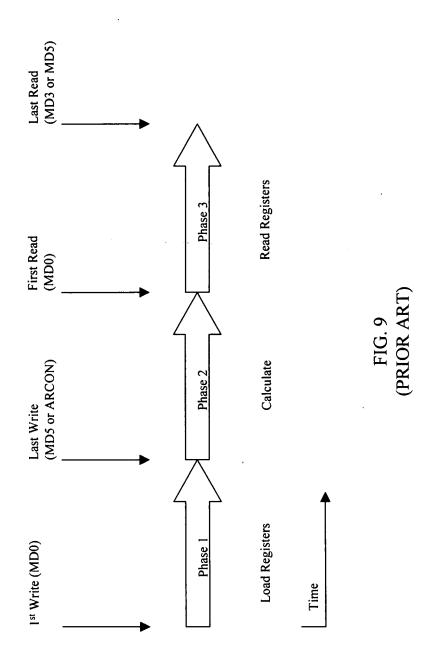












Operation	Result	Remainder	Execution Time
32-bit/16-bit	32-bit	16-bit	6 tcy
16-bit/16-bit	16-bit	16-bit	4 tcy
16-bit x 16-bit	32-bit	-	4 tcy
32-bit normalize	•	•	6 tcy
32-bit shift left/right	1	1	6 tcy

### Notes:

- 1) 1 tcy = 1 microsecond at 12 Mhz Oscillator frequency
- 2) The maximum shift speed is 6 shifts per machine cycle

FIG. 10 (PRIOR ART)

	7	9	S	4	3	2	-	0	
	MDEF	MDEF MDOV SLR	SLR	SC.4	SC.4 SC.3 SC.2 SC.1	SC.2	SC.1	SC.0	
	MDEF = Error flag  1 = Indicates an improperation, MDEF is s	MDEF = Error flag  I = Indicates an improperly performed operation. MDEF is set by hardware	erly perforn by hardwar	peu	SLR 1 = S 0 = S	SLR = Shift Right or Shift Left 1 = Shift Right 0 = Shift Left	ht or Shift	Left	
	when an operati write access bef operation has be 0 = Reset value.	when an operation is retriggered by a write access before the previous operation has been completed.  0 = Reset value.	riggered by previous pleted.	a	CNT4 Shift C When Select Shift C	CNT4,CNT3,CNT2,CNT1,CNT0 Shift Counter When preset with 00000b, normalizing is Selected. When set with values other than Shift operation is selected.	CNT1,CNT0 000b, normaliz vith values othe	CNT4,CNT3,CNT2,CNT1,CNT0 Shift Counter When preset with 00000b, normalizing is Selected. When set with values other than 00000b, Shift operation is selected.	
L	MDEF = Overfile Exclusively controlivision by zero multiplication when the multiplication we have a sero exclusion and the sero exclusion and exclusion and exclusion are exclusively and exclusion are exclusively and exclusive exclusion and exclusive exclus	MDEF = Overflow flag  Exclusively controlled by hardware. MDOV is set by following events: -division by zero - multiplication with result greater than 0FFFFh	/ hardware.	MDOV is s	et by follow	ing events:			

FIG. 11 (PRIOR ART)

0 = Reset value.

12/14

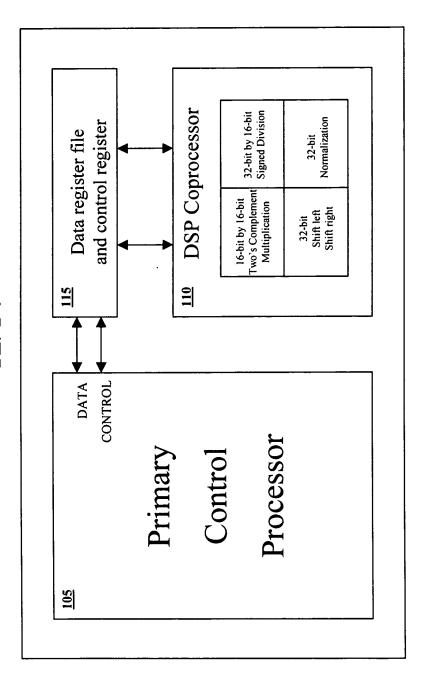
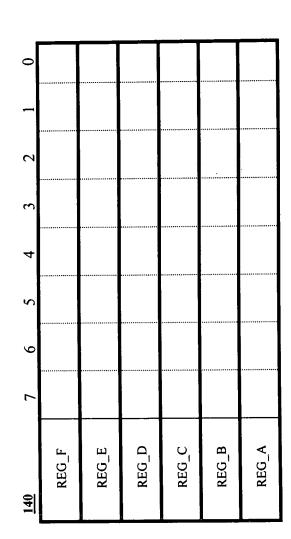


FIG. 12

		-			
0	CNT0		Left	ation	
-	CNT1		ight or Shift	,CNT1,CNT0 iR or Normaliza	
2	MO SLSR CNT4 CNT3 CNT2 CNT1 CNT0		SLSR = Shift Right or Shift Left 1 = Shift Right 0 = Shift Left	CNT4,CNT3,CNT2,CNT1,CNT0 Shift Count for SLSR or Normalization Input for SLSR Output for Normalization	
3	CNT3	130	SLS 1 = 0	CN1 Shift Inpu	135
4	CNT4			J	
5	SLSR		uc	oit divide oit multiply peration lization	
9	МО		Operation	<ul> <li>0 32-bit by 16-bit divide</li> <li>1 16-bit by 16-bit multiply</li> <li>0 32-bit Shift operation</li> <li>1 32-bit Normalization</li> </ul>	
120 7	M1	125	M1 M0	0 - 0	

FIG. 13



145

DIVISION = (REG\_F,REG\_E,REG\_D,REG\_C) (REG\_B,REG\_A)

QUOTIENT = (REG\_F, REG\_E, REG\_D, REG\_C)

REMAINDER = (REG\_B,REG\_A)

145

MULTIPLICATION = (REG\_D,REG\_C) X (REG\_B,REG\_A)
PRODUCT = (REG\_D,REG\_C,REG\_B,REG\_A)
REG\_F, and REG\_E are unused

145

SHIFT LEFT, SHIFT RIGHT & NORMALIZATION (REG\_D,REG\_C,REG\_B,REG\_A)
REG\_F, and REG\_E are unused

FIG. 14